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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,421	06/30/2003	Volkan Kursun	000687-00302	8087

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 02/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,421	KURSUN ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18,26,34,42,50 and 51* is/are pending in the application.

4a) Of the above claim(s) *19-25,27-33,35-41 and 43-49* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18,50 and 51* is/are rejected.

7)☒ Claim(s) *26, 34, 42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Newly submitted claims 27-33, 35-41, 43-49 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: the claimed subject matters are directed to a bias generating circuit that is non-elected invention.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 27-33, 35-41, 43-49 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Krishnamurthy et al (6,346,831).

Krishnamurthy shows:

1. a domino logic circuit (Fig. 6, 7, 8) comprising: a pulldown circuit having a dynamic node (Q, Fig. 7; A, Fig. 6); a keeper (M16, M24) connected to the pulldown circuit at the dynamic node; and a source (174) of a body bias voltage, the source of the body bias voltage being connected to the keeper to supply the body bias voltage (Vbbn) to the keeper to bias the keeper.

2. The domino logic circuit of claim 1, wherein the body bias voltage is a reverse body bias voltage (col. 4, lines 45-52).

3. The domino logic circuit of claim 2, wherein the reverse body bias voltage is static (constant, col. 4, line 49).

4. The domino logic circuit of claim 3, further comprising a foot transistor (M20, Fig. 6) for connecting the pulldown circuit to ground.

5. The domino logic circuit of claim 3, wherein the pulldown circuit is connected to ground without an intervening foot transistor (112, Fig. 7).

6. The domino logic circuit of claim 2, wherein source supplies the reverse body bias voltage such that the reverse body bias voltage alternates between two values (changing voltages, col. 4, line 49).

7. The domino logic circuit of claim 6, further comprising a foot transistor (M20, Fig. 6) for connecting the pulldown circuit to ground.

8. The domino logic circuit of claim 6, wherein the pulldown circuit is connected to ground without an intervening foot transistor (112, Fig. 7).

9. The domino logic circuit of claim 1, wherein the body bias voltage is a forward body bias voltage (col. 7, lines 20-36).

10. The domino logic circuit of claim 9, wherein the forward body bias voltage is static (constant, col. 4, line 49).

11. The domino logic circuit of claim 10, further comprising a foot transistor (M20, Fig. 6) for connecting the pulldown circuit to ground.

12. The domino logic circuit of claim 10, wherein the pulldown circuit is connected to ground without an intervening foot transistor (112, Fig. 7).

13. The domino logic circuit of claim 9, wherein source supplies the forward body bias voltage such that the forward body bias voltage alternates between two values (changing voltages, col. 4, line 49).

14. The domino logic circuit of claim 13, further comprising a foot transistor (20, Fig. 6) for connecting the pulldown circuit to ground.

15. The domino logic circuit of claim 13, wherein the pulldown circuit is connected to ground without an intervening foot transistor (112, Fig. 7).

16. The domino logic circuit of claim 1, wherein source supplies the body bias voltage such that the body bias voltage alternates between a first forward body bias voltage value and a second reverse body bias voltage value (changing voltages, col. 4, line 49).

17. The domino logic circuit of claim 16, further comprising a foot transistor (20, Fig. 6) for connecting the pulldown circuit to ground.

18. The domino logic circuit of claim 16, wherein the pulldown circuit is connected to ground without an intervening foot transistor (112, Fig. 7).

50. The domino logic circuit of claim 1, wherein the body bias voltage has a value which is selected for noise immunity (in many cases, performance and noise immunity are traded off, col. 7, lines 2-22).

51. The domino logic circuit of claim 1, wherein the keeper has a size which is selected for noise immunity (M16, col. 4, lines 47-53, also, Fig. 6 is similar to circuit 50 in Fig. 3, col. 7, line 22-23).

Allowable Subject Matter

3. Claims 26, 34, & 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter: two voltage values alternate in accordance with an operational phase of the domino logic circuit.

Response to Arguments

5. Applicant's arguments filed 12/03/04 have been fully considered but they are not persuasive. Applicant argues that "The applied reference is silent on any reasons for body-biasing the keeper". The applied reference teaches bias generation circuitries may provide bias voltage to PFETs and NFETs transistors of Figs 6, 7, and 8 to increase Vt and decrease leakage and increase noise immunity (col. 7, lines 45-57). Therefore, the applied reference teaches body-biasing the Keepers M16, M24, and M33 (PFETs) of Figs 6, 7, and 8 for decrease leakage and increase noise immunity.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

2/8/05

ANH Q. TRAN
PRIMARY EXAMINER